REMARKS/ARGUMENTS

Claims 1-10 and 12-20 are currently pending in the present patent application, with claim 11 having been cancelled through the above claim amendments.

In a final Office Action mailed October 18, 2006, the Examiner maintained the rejection of claims 1 and 4 under the second paragraph of 35 U.S.C. § 112 as containing antecedent basis problems noted by the Examiner. These claims have been amended to eliminate these antecedent basis problems so the rejection of these claims on this basis should be withdrawn.

In Section 5a of the final Office Action, the Examiner maintains his rejection of claim 8 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent Application Publication No. 2002/0087817 A1 to Tomaiuolo ("Tomaiuolo"). The Examiner reasons that the disclosed memory device is accessible sequentially wherein the access takes place by successive locations and that the subsequent memory location to be read, and therefore its address is predictable (i.e., predetermined) from the address of the location being currently read.

Claim 8 recites, in part, a control circuit coupled to the memory locations and operable to allow sequential access to the contents of the memory locations via a predetermined one of the memory locations during a second mode of operation. This language plainly and unambiguously recites that the contents are accessed "via a predetermined one of the memory locations." This predetermined one of the memory locations is the same memory location that is always used for accessing the memory contents in this mode. Tamaiuolo neither discloses nor suggests using the same predetermined location to sequentially access memory locations via this same predetermined or selected memory location. The operation of Tamaiuolo discussed by the Examiner may be viewed as a type of burst mode of operation and does correspond to the express language of claim 8, namely "sequential access to the contents of the memory locations via a predetermined one of the memory locations."

The combination of elements recited in amended claim 8 is accordingly allowable and dependent claims 9 and 10 are allowable for at least the same reasons as claim 8 and due to the additional limitations added by each of these claims. Independent claims 14 and 15 and dependent claims 16-20 are allowable for reasons similar to those just discussed with regard to claim 8.

The Examiner also maintained his rejection of claims 1-7 as being obvious over U.S. patent 6,091,645 to Iadanza ("Iadanza") in view of Applicants Admitted Prior Art ("APA").

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· Claim 1 recites, in part, a memory including at least one array of memory elements, with the at least one array being partitioned into a plurality of sub-arrays of the memory elements and an array configuration circuit that selectively puts the at least one array in one of two operating configurations. The second operating configuration is such that the memory elements in each sub-array are coupled to one another so as to form an independent monodimensional sequentially-accessible memory block, a data content of any memory element of the sub-array being rotatable by shifts through the memory elements of the sub-array.

As the Examiner describes in Section 5b of the Office Action, Iadanza discloses a memory wherein each sub-array comprises a plurality of memory cells 48 arranged in an array of M rows and N columns. Each memory cell 48 of the first row and first column has an associated transfer cell 50 that enables shifting of data vertically from word to word. In this same section the Examiner states that when data is pushed into a given sub-array, overflow data is shifted out of the given sub-array and propagated to the next adjacent sub-array. From this description, it is seen that in Iadanza as data is pushed into a given sub-array the content of the next sub-array is dependent on the content of the previous sub-array.

This operation is contrary to the express language of claim 1. Claim 1 expressly recites that "the memory elements in each sub-array are coupled to one another so as to form an independent monodimensional sequentially–accessible memory block, a data content of any memory element of the sub-array being rotatable by shifts through the memory elements of the sub-array." Each sub-array is an independent sequentially-accessible memory block. Each sub-array is independent of the other sub-arrays, as is seen, for example, in Figure 4 (see discussion in prior amendment regarding this figure) of the present application. When the recited memory operates according to the second operating configuration, data is rotated among the memory elements of each sub-array independently, and not from one sub-array into another sub-array. The Examiner's interpretation of this language in claim 1 effectively eliminates the word "independent" from the claim language. This is not a reasonable interpretation of this language." With the Examiner's interpretation, what is the difference between the phrase "independent monodimensional sequentially-accessible memory block" and "monodimensional sequentially-accessible memory block"?
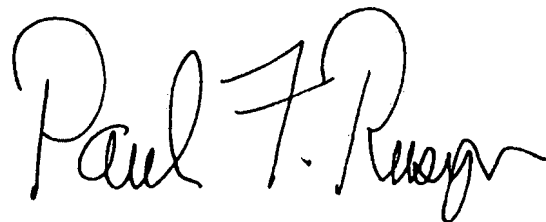
The combination of elements recited in claim 1 is therefore allowable and dependent claims 2-7 are allowable for at least the same reasons as claim 1 and due to the additional limitations added by each of these claims.

Claim 12 has been rewritten in independent form to recite, in part, a memory, including an array of memory locations and a control circuit coupled to the array and operable to cause the array to operate as a random access memory during a first mode of operation and a first in first out memory during a second mode of operation, wherein the memory locations comprise rings of serially coupled memory locations each having a respective contents, with the contents of each ring being independent of the contents of the other rings. Neither Iadanza nor the APA, whether taken singly or in combination, disclose or suggest such rings of memory locations as recited in amended claim 12. The combination of elements recited in claim 12 is therefore allowable and claim 13 is allowable for at least the same reasons as claim 12 and due to the additional limitations added by claim 13.

The present patent application is in condition for allowance. Favorable consideration and a Notice of Allowance are respectfully requested. Should the Examiner still consider any of the claims not allowable, the undersigned respectfully requests the Examiner to contact him at (425) 455-5575 to arrange for a telephone interview to discuss the Examiner's issues with the claims. If the need for any fee in addition to that paid with this response is found, for any reason or at any point during the prosecution of this application, kindly consider this a petition therefore and charge any necessary fees to Deposit Account 07-1897.

Respectfully submitted,

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